TEMIC 51T (Temic) EMULATION

Note:

To use with frequencies above 40Mhz it will be required to use an emulator board that has been specially modified to obtain high frequency operation and will work **only** with the POD-51Temic. The EPROM on the emulator board must be version COM 1.4. If running in X2 mode above 18Mhz or 36Mhz in X1 mode you will require the CBL-18 (18 inch) cable instead of the normal 5' (5 foot) cable.

The solder side of the board has a 44-pin PGA plug. The plug goes into the target system via a 44 pin PGA to 44 pin PLCC, or 44-pin QFP adapter (*To be ordered separately*).

The pod has five LEDs, named MON, EMUL, PD, IDLE, RES:

- MON – is red, and means that the system is in monitor mode. In monitor mode, the processor is executing code that is internal to the emulator. This code is not user code, and is used to communicate with the host PC to set up breakpoints, etc.

- EMUL – is green, and means that the system is in emulation mode. In emulation mode, the processor is executing the user's code from the emulation RAM or the target's PROM depending on the mapping in the emulator software.

- PD – is yellow, and means that the microcontroller is in the *Power-down* state.

- IDLE – is yellow, and means that the microcontroller is in the *IDLE* state.

If you break emulation during either the Power-down or Idle states, the emulator will lose control of the system and the emulation software will yield an error condition. RESET is the only way to regain control of the microcontroller and emulator again.

- RES – is red, and means that the microcontroller RESET pin is LOW (active state).

JP5 determines the mode(s) of operation for this pod board:

Jumper ID	IN/ OUT	Default	Description of function
M1 [*1]	**IN** **OUT**	**BASED ON MICRO**	Installed for 80 and 87 series microcontrollers and Removed for 89 series microcontrollers.
M2, M3, M4	**IN** **OUT**	**(see table 2)**	Select memory size based on microcontroller installed
M5	**IN** **OUT**	**OUT**	Reset Address for Boot-loading if the jumper is installed. [*2] If removed, then use SLOW timing. [*3]
M6	**IN** **OUT**	**OUT**	If installed, then disable all clock-based peripherals in Monitor mode.
M7	**IN** **OUT**	**IN**	If installed, PSEN is gated. If removed, PSEN is not gated.
M8	**IN** **OUT**	**OUT**	If installed, then writes to SFRs (special function registers) will be traced.

(*1) See table 2 for initial memory configurations.
(*2) F800h, but may differ based on installed mcu.

(*3) If M1 is IN and M5 is OUT, then Fast Bus timing is selected, to be used with frequencies above 40Mhz).

Table 1

			89 Series (flash)		80 & 87 Series	
M2	**M3**	**M4**	**ROM**	**XRAM** *4	**ROM**	**XRAM**
Out	**Out**	**Out**	0 K	0	0 K	0
Out	**Out**	**In**	4 K	0	4 K	0
Out	**In**	**Out**	8 K	0	8 K	0
Out	**In**	**In**	12 K	0	16K	0
In	**Out**	**Out**	16 K	256	16K	256
In	**Out**	**In**	20 K	0	32 K	0
In	**In**	**Out**	32 K	256	32 K	256
In	**In**	**In**	64 K	768	64 K	768

(*4) Initial starting XRAM size. The size can be adjusted by the microcontroller's AUXR register.

Table 2

The board has three jumpers for power and crystal connection to the emulation chip:

- PWR – is used to select power for the processor. Power should be supplied from the emulator and the jumper should be in either the **5v** or **3v** position depending on the type of microcontroller installed in the pod. With the power jumper in the left two pins (**EXT** position), then the power will come from the target system.

- XTAL – determines if the crystal or clock is taken from the target system or the on pod crystal**.** The jumpers should be in the top two positions for crystal to be supplied from the pod or the **INT** position. If the jumpers are in lower positions (**EXT** position), then the crystal/clock is supplied from the target system.

If you use an external clock, note that XTAL1 is an input and XTAL2 is left open.

All jumpers for PWR should be in the **5v** or **3v** position depending on the type of microcontroller installed position and XTAL will be in the **INT** position when no target is connected to the pod board.

RST connects the target RESET pin to the emulator. If the target system has a watchdog, it will probably interfere with the emulation and **RST** should then be removed.

JP2 is used to connect external signals to the emulator. They are used for trace function. The pin to the right (away from the Pod's cable connector) is **SY1**. The name of the pin in the center is **SY0** and can also be used in the breakpoint logic. The pin on the left (closest to the pod cable connector) is the **EM/** signal. This signal goes low during the RUN mode and goes high when you enter monitor mode of the emulator.

JP1 is used to connect the bank switch signals to the emulator boards bank switching memory logic. These lines are only used if you are using bank switching with your application and target. Each of these pins is an input to the banking logic, and used to jumper to the target system's latched banking logic

lines. There are only 4 input banking lines that can be used; they are labeled on the J1 as BSW0, BSW1, BSW2, and BSW3 (10K pull-up). The pins labeled SFR and MOVX are currently not defined, and you should not connect anything to these pins.

The header labeled FLF/, ANB/ carries signals from the emulator. The ANB/ pin is used in conjunction with the Enhanced Trace boards as a signal output from a state machine logic. The **B0/** and **B1/** jumpers are used to complete the connection of the BSW0 and BSW1 lines to the emulator's bank logic.

Jumper P1/P0 upper pins carry the processor port 1 pins in order with P1.0 on the left, and P1.7 on the right. Port 1 is connected directly to the processor. The lower pins carry port 0 with P0.0 on the left and P0.7 on the right. Port 0 is emulated in the FPGA. This means that the P0 has better sink capability than the processor. Output signals also appear three clock cycles later than the real part. The middle row of the jumper P1/P0 is normally connected to P1 using the jumpers. The signal level on the middle pins will be reflected on the trace display. The board is delivered with the jumpers installed so that P1 will be traced. External signals can be connected to the middle pins if the jumpers are removed. The input load is a 100K pull-up.

Jumper P2/P3 upper pins carry the processor port 3 pins in order with P3.0 on the left, and P3.7 on the right. Port 3 is connected directly to the processor, except for P3.6 & P3.7 that go through a high speed logic switch and carries approx. 100 ohms of series resistance. The lower pins carry port 2 with P2.0 on the left and P2.7 on the right. Port 2 is emulated in the FPGA. This means that the P2 has better sink capability than the processor. Output signals also appear three clock cycles later than in the real part.

The Middle row of the jumper P2/P3 is normally connected to P3 using the jumpers. The signal level on the middle pins will be reflected on the trace display. The board is delivered with the jumpers, so that P3 will be traced. External signals can be connected to the middle pins if the jumpers are removed. The input load is a 100K pull-up.

S1 push-button is used to reset the processor, and can be used instead of a target system reset.

Note:

Ports 0 and 2 are emulated, and have a slightly different AC and DC characteristics:

> Emulated I/O pins sink a minimum of 4 mA, and source (P2) minimum 4 mA for two clock cycles after an output low to high transition. As high outputs or inputs, P2 ports have 22 kohm pull-up resistors.
>
> Emulated output will change state three clock cycles later than a normal output would.

P3.6 and P3.7 go through a high speed switch logic which adds approx. 100 ohms to their output impedance.

When accessing target memory, P0, and P2 will be delayed approximately 5-10 ns.

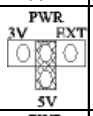
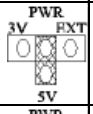
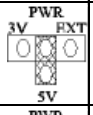
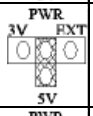
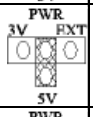
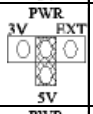
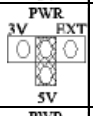
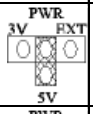
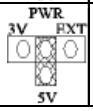
The timer/counters are stopped at breakpoints. This usually means that the serial port also stops at breakpoints. If a character is received or sent at this moment, it will be distorted.

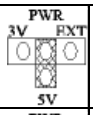
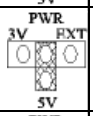
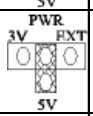
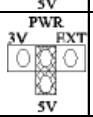
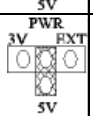
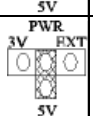
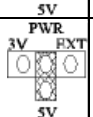
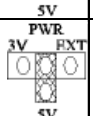
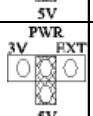
If you break emulation during the time that the PD (power-down) or IDLE leds are lit, a number of communication errors will cause the software to lose control of the emulation system. The system will have to be restarted at this point.

Connecting the pod board to the target system:

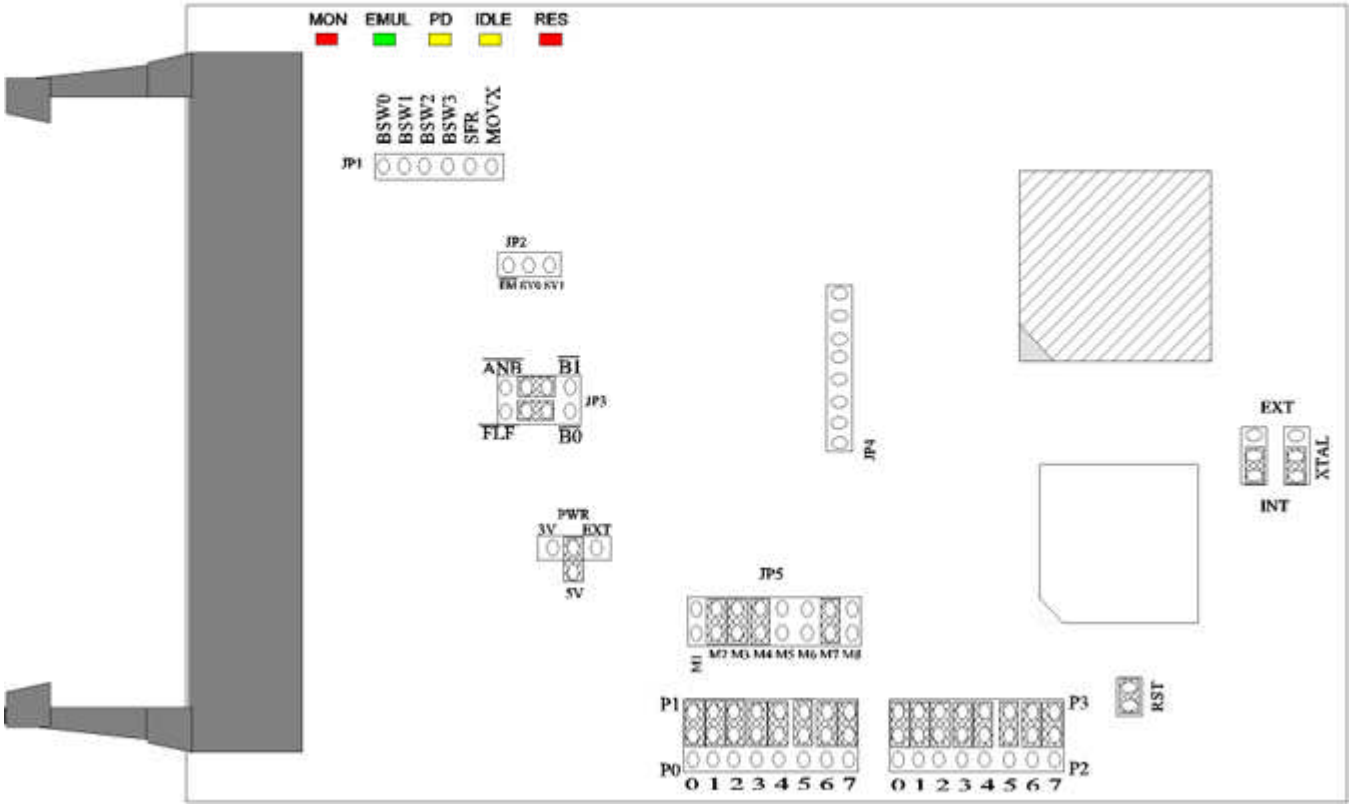
Make sure that the power is turned off to both the emulator and the target system. Connect the black ground wire to the target first to assist in discharging any static electricity. Now you may connect the pod to the processor connection, and power up both the emulator and target systems.

If you have the jumper for power selected for target, you should power up the target first, then the emulator, or both together. If selected for internal power, then power up the emulator first, then the target. Power-down in the reverse sequence.

Installed	**Jumpers M1 thru M8 X = Installed**										
MCU	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**PWR**	**P0 / P1**	**P2 / P3**
8031, 8032, 8051, 8052, 8031x2, 8032x2, 8054,8058	X				X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8751	X			X	X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8752	X		X		X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8754	X	X			X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8758	X	X	X		X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8951, 89S51				X	X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8952, 89S52, 8952X2			X		X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8953			X	X	X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8954, 8954X2		X			X	X	X			Install all on the P1 (top)	Install all on the P3 (top)

8958		X	X		X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8051RA	X	X			X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8051RB,8751RB, 8751RB2	X	X			X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8051RC,8751RC, 8751RC2	X	X	X		X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8051RD,8751RD, 8751RD2	X	X	X	X	X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8951RB, 8951RB2					X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8951RC, 8951RC2		X	X		X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8951RD, 8951RD2, 89C51ED2		X	X	X	X	X	X			Install all on the P1 (top)	Install all on the P3 (top)
8751U2	X		X	X	X	X	X			Install all on the P1 (top)	Install all on the P3 (top)

POD-51T
Jumpers & Headers



– *Figure 1* – Jumpers and Headers