## nohau

HSP

# **EMUL-AVR-PC** User Guide



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## **EMUL–AVR–PC**<sup>™</sup>

#### **User Guide**

Edition 1, July 24, 2001

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Sales Offices, Representatives and Distributors

#### **Product Notes**

#### **Warranty Information**

The emulator board, trace board, pod board, and emulator cable are sold with a one-year warranty starting from the date of purchase. Defective components under warranty will either be repaired or replaced at Nohau's discretion.

Pod boards that use a bondout processor are also warranted for one year from the date of purchase except for the processor. The bondout processor will be replaced once if Nohau determines that the failure in the bondout processor was not due to the user's actions. This replacement limit does not apply to the rest of the pod board.

Each optional adapter, cable, and extender is sold with a 90-day warranty, except that it may be subject to repair charges if damage was caused by the user's actions.

Nohau's Seehau software is sold with no warranty, but upgrades can be obtained to all customers at the Nohua Web site: <u>http://www.nohau.com</u>.

Nohau makes no other warranties, express or implied, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose. In no event will Nohau be liable for consequential damages. Third-party software sold by Nohau carries the manufacturer's warranty.

#### **European CE Requirements**

Nohau has included the following information in order to comply with European CE requirements.

#### **User Responsibility**

The in-circuit debugger application, as well as all other unprotected circuits need special mitigation to ensure Electromagnetic Compatibility (EMC).

The user has the responsibility to take required measures in the environment to prevent other activities from disturbances from the debugger application according to the user and installation manual.

If the debugger is used in a harsh environment (field service applications for example), it is the user's responsibility to control that other activities cannot be disturbed in such a way that there might be risk for personal hazard/injuries.

#### **Special Measures for Electromagnetic Emission Requirements**

To reduce the disturbances to meet conducted emission requirements it is necessary to place a ground plane on the table under the pod cable and the connected processor board. The ground plane shall have a low impedance ground connection to the host computer frame. The insulation sheet between the ground plane and circuit boards shall not exceed 1mm of thickness.

#### System Requirements

#### CAUTION

Like all Windows applications, the Seehau software requires a minimum amount of free operating system resources. The recommended amount is at least 40%. (This is only a guideline. This percentage might vary depending on your PC.) If your resources are dangerously low, Seehau might become slow, unresponsive or even unstable. If you encounter any of these conditions, check your free resources. If they are below 40%, reboot and limit the number of concurrently running applications. If you are unable to free at least 40% of your operating system resources, contact your system administrator or Nohau Technical Support at support@nohau.com.

The following are minimum system requirements:

- Pentium 200 (Pentium II or faster is recommended)
- Single-Processor System
- Windows 95, 98, ME, NT, 2000 Pro
- Random Access Memory (RAM)
  - For Windows 95, 98, ME: 64 MB
  - For Windows NT/2000 Pro: 128 MB

#### **About This Guide**

#### **Basic Tasks**

The *EMUL–AVR–PC User Guide* describes how to use the EMUL–AVR–PC emulation system with the Seehau graphical user interface. This guide is intended for both novice and advanced users.

The EMUL–AVR–PC is a PC-based emulator for the Atmel AT90 AVR family of microprocessors. This guide helps you to get started with the basics of setting up, configuring, and running the Seehau software and the emulator. If you have any questions contact Nohau Technical Support at support@nohau.com or refer to the Sales Offices, Representatives and Distributors list at the end of this guide.

Online context sensitive Help is also available from the Seehau software by pressing the F1 or the Help keys, depending on the type of keyboard you have.

The EMUL-AVR-PC User Guide introduces the following tasks:

- Installing and Configuring the Communications Interface
- Installing the ISA Plug-In Board and EPC with Windows
- Installing and Configuring the Emulator Hardware
- Installing and Configuring the Seehau Software
- Using Adapters and Flex Cables
- Running Time Program Examples
- Configuring Trace Triggers
- Troubleshooting

#### **Downloading EMUL-AVR-PC Product Documentation**

To download an electronic version of this guide, do the following:

- 1. Open Nohau's home page at www.nohau.com.
- 2. Click Publications.
- 3. Click Nohau Manuals.
- **4.** Scroll down to EMUL–AVR–PC. Then select EMUL–AVR–PC to download a PDF version of this guide.

### Overview of the EMUL-AVR-PC Emulator System

#### Features

The EMUL–AVR–PC system provides real-time emulation for both single-chip and external modes and includes the following:

- Communications interface
  - Emulator Parallel Cable (EPC)—Requires a printer port connection (LPT).
  - ISA card—Requires an 8-bit ISA slot.
- Emulator pod board
- Adapter to connect to your target system

#### **User Interface**

The emulator is configured and operated by the Seehau user interface. Seehau is a high-level language user interface that allows you to do the following tasks:

- Load, run, single-step and stop programs based on C or Assembly languages.
- Set triggers and view trace.
- Modify and view memory contents including SFRs.
- Set software and hardware breakpoints.

## **2** Installing and Configuring the Communications Interface

#### **Communications Interfaces**

To operate the EMUL–AVR–PC Emulator System, you must use one of the following communications interfaces to connect the emulator board:

- Emulator Parallel Cable (EPC)—Communicates with the emulator system through a standard PC parallel port (LPTx).
- LC–ISA Plug-In Board—Requires an 8-bit ISA slot. Includes a cable that connects the ISA board to the emulator board.

For detailed instructions on how to install the LC–ISA plug-in board or the EPC with Windows NT, 2000 Pro or Window 95/98/ME, refer to the Windows NT/2000 Pro and Windows 95/98/ME installation instructions later in this chapter.

#### **Emulator Parallel Cable (EPC)**

The EPC allows you to connect to a standard PC parallel port and communicate with the AVR emulator (Figure 1). Figure 2 shows both ends of the cable: the male side connects to the PC, and the female side connects to the printer.



Figure 1. Emulator Parallel Cable



Figure 2. EPC Connectors

#### **LC-ISA Plug-In Board**

The EMUL/LC–ISA board is an 8-bit PC card that fits into any ISA slot (Figure 3). The jumpers on the emulator board control three things:

- The address used to communicate with the Host PC
- The maximum PC clock communication rate to the target
- Whether or not power is provided to the target through the LC connector.



Figure 3. LC–ISA Board

#### Installing the LC-ISA Board

When installing the LC-ISA Board, check the following items:

- Check the I/O address jumpers.
- Verify the target communication rate.
- Check to ensure the JP2 PWR power jumper is removed.

#### Check the I/O Address Jumpers: J1

#### Note

The factory default is set at 200 for the software and hardware. Refer to the Windows NT and Windows 95/98 installation instructions later in this chapter to determine if this default address will conflict with your existing PC hardware.



Factory Default





Figure 5. Alternate Address Settings for Header J1

Set the emulator board address using the jumpers in header J1. The EMUL/LC–ISA requires eight consecutive I/O addresses from the PC's I/O address space (0 hex - 3FF hex) that begin on an address that is a multiple of eight. These addresses must not conflict with any other I/O device.

Each pair of pins in J1 represents one bit in the 10-bit address. Address bits 0, 1, and 2 represent addresses within the eight consecutive addresses and do not have pin pairs to represent them. This leaves seven address bits (pin pairs) to set with jumpers. Shorting pins represents a 0 (zero)in the address. A pair of pins with no jumper represents a 1. Figure 5 shows four examples where the Least Significant Bit (LSB) is on the left and the 25-pin D connector is on the right.

#### Verify the Target Communication Rate: Header JP1

The communication clock rate is divided by moving the jumper on JP1.

Refer to Figure 6 to set the fixed synchronous communication rate. Note the clock rate in the lower row. Place one jumper on the header JP1 between the pins indicated in the upper row. Make sure only one jumper is connected to this header.

#### Note

The pins on header JP1 are not numbered on the board.

Figure 6 shows the orientation of JP1 as it appears on the emulator board. In Figure 6, the pin 1 hole is shown as a square as it is on the emulator board.

#### Note

The default position shown in Figure 6 should work for most computer applications. However, if you experience a communications problem, move the jumper one or two positions to the right.

#### PWR Header—JP2

This jumper should be removed.

Short These Pins	1, 2	3, 4	5, 6	7, 8	9, 10	11, 12	13, 14	15, 16	17, 18	
	0	0	0	0	0	0	0	0	0	
		0	0	0	0	0	0	0	0	
CLKOUT Rate	8.3 MHz J	4.2 MHz	2 MHz	1 MHz	524 KHz	262 KHz	131 KHz	65 KHz	32 KHz	

Figure 6. Default Position for Header JP1

#### Installing the ISA Plug-In Board and EPC with Windows

This section describes Windows NT/2000 Pro and Windows 95/98/ME installation procedures for the ISA plug-in board and the EPC.

#### Installing the ISA Plug-In Board with Windows NT

To install the ISA plug-in board, check the following items:

- Check whether you have administrative privileges to install Nohau software under Windows NT.
- Check for possible conflicts with your PC and the default address range for the LC–ISA card.

#### Checking Administrative Privileges

To check whether you have administrative privileges, do the following:

- 1. Click the Start menu, and select Programs.
- 2. Select Administrative Tools, and click User Manager. The User Manager dialog box opens.
- **3.** In the bottom half of the dialog box, double-click **Administrators**. The **Local Group Properties** dialog box opens with a list of login names.
- **4.** Look for your login name in the list of names. If your login name is not present, you are not set up with administrative privileges. Contact your System Administrator to update your privileges or give you the administrator's password.

#### Checking Your PC for Conflicts with the Default Address Range

The default address range for the LC–ISA card is 200H to 207H. You will need to check your PC for possible conflicts with this default.

- 1. Click the Start menu, and select Programs.
- **2.** Select Administrative Tools, and click Windows NT Diagnostics. The Windows NT Diagnostics screen appears.
- **3.** Click the **Resources** tab.
- 4. Click the I/O Port button.
- 5. Check the I/O resources listed to make sure there is no device in the default address range.

If you see a device present in that range, look for an alternate address. Start at address 100H. Look for a range in multiples of eight with no device present. For example, the base address must be an even multiple of eight (such as 200 or 208). If you have to change the address of the emulator, make sure you change both the jumpers on the board and the software settings.

After installation, Windows NT Diagnostics will show the NohauAVR device driver present in the upper I\O range (FFxx). After launching Seehau, the driver is reassigned to the actual address range. In the Control Panel Devices window, you will see three columns: Device, Status, and Startup.

- Device—Lists the Nohau device driver
- Status—Displays Started
- Startup—Displays Automatic

#### Troubleshooting

- If you get a Service or driver failed error upon reboot, you probably have a resource conflict.
- If you get a **create file failed** error message upon execution, the device driver did not properly start. Review the steps in this section again. You can use Windows NT Diagnostics to recheck that your port address has no conflicts.

#### Installing the ISA Plug-In Board with Windows 95/98/ME

The default address range for the LC–ISA card is 200H to 207H. You will need to check your PC for possible conflicts with this default by doing the following:

- 1. Click the Start menu, and select Settings.
- 2. Click Control Panel.
- **3.** Double-click **System**. The System Properties window opens.
- 4. Click the Device Manager tab.
- 5. Click the Properties button.
- **6.** Click the Input/output button. Scroll the contents of the window to make sure there is no device in that range.

If you see a device present in the default range, look for an alternate address. Start at address 100H and look for a range in multiples of eight with no device present. For example, the base address must be an even multiple of eight (such as 200 or 208). If you have to change the address of the emulator, be sure to change both the jumpers on the board and the software settings.

#### Installing EPC with Windows NT/2000 Pro

#### Checking Administrative Privileges

You must have administrative privileges to install Nohau software under Windows NT/2000 Pro.

To check whether you have administrative privileges, do the following:

- 1. Click the Start menu, and select Programs.
- 2. Select Administrative Tools, and click User Manager. The User Manager dialog box opens.
- **3.** In the bottom half of the dialog box, double-click **Administrators**. The **Local Group Properties** dialog box opens with a list of login names.
- **4.** Look for your login name in the list of names. If your login name is not present, you are not set up with administrative privileges. Contact your System Administrator to update your privileges or give you the administrator's password.

#### Troubleshooting

- If you get a **Service or driver failed** error when rebooting, you probably have a resource conflict.
- If you get a **create file failed** error message upon execution, the device driver did not properly start.

## **3** Installing and Configuring the POD-AVR

The POD–AVR is designed to emulate the Atmel AT90 AVR microcontroller family. Both hardware jumpers and software configure the pod board. For details on configuring the Seehau software, see Chapter 5, "Installing and Configuring the Seehau Software."

#### **Cable Connection**

The DB25 connector is used to communicate with the host computer. Two methods are available:

- The Enhanced Parallel Cable (EPC) connects through the parallel port.
- The LC–ISA cable connects through an adapter board mounted on the ISA back plane.

#### **Jumper Default Positions**

Jumpers are configured for stand-alone operation rather than target operation. Figure 7 shows the jumpers in the default positions.





#### **Jumper Descriptions**

Jumper Designation	Function	Description
JP1	AVR Power	This jumper selects the source of power to the AVR bondout chip.
		<ul> <li>Installed in the Pod position—Vcc is 5V from pod for stand-alone emulator.</li> </ul>
		<ul> <li>Installed in the Target position—Vcc from the target pin.</li> </ul>
JP2, JP3	Clock	These jumpers determine the clock source.
		<ul> <li>Installed in the Pod position—Pod clock generator.</li> </ul>
		<ul> <li>Installed in the X position—External source from the target or the Tiny12 internal clock.</li> </ul>
JP4	EPC Power	This jumper indicates connection for +5V power for the EPC.
		• Installed—EPC cable is used.
		• Open—LC–ISA card is used.
JP6	Analog Power	Determines the power source for analog circuitry and digital ports on some CPUs.
		• Installed in the AVR Vcc position—Source is Vcc to AVR from JP1.
		<ul> <li>Installed in the Target Avcc position—Source is Avcc pin on the target adapter.</li> </ul>

#### **Connector Descriptions**

Connector Designation	Function	Description
J7	Pod Power Input	The pod is powered by a +5VDC Nohau power pack plugged into the J7 power jack.
JP5	Misc Trace Inputs	Connects optional signals from the target. Pins $1 - 8$ correspond to bits $0 - 7$ , pins 9, and 10 are ground (GND). (See Figure 8.)
J3	Communication Interface	The EPC plugs into the pod through this DB-25 connector and is powered by the power pack when the JP4 jumper is installed.



Figure 8. Miscellaneous Trace Inputs Pins on JP5

Designation	Function	Description
TP1	TP1	For factory use only
TP2	TP2	For factory use only
ТР3	GND	Ground reference
TP4	XTRIG_IN	External trigger input
TP5	XTRIG_OUT	External trigger output
TP6	GND	Ground to target. To prevent static discharge damage, attach this first.

#### **Test Point Descriptions**

#### **LED Indicators**

Designation	Function	Description
LED3	LOGIC	Red indicates logic is not loaded. Green indicates the logic is loaded.
LED4	RESET	On indicates a RESET is occurring (an active reset condition). Possible sources include:
		Seehau User Interface
		Target Reset Circuit
LED5	RUN	Red indicates the emulator is running in the Monitor mode. Green indicates the user code is running (except during reset).
LED6	AVR Power	On indicates the Vcc to AVR is active.

## Installing and Configuring the Seehau Software

#### **Installing Seehau**

To install the Seehau software, do the following:

- 1. Locate your Seehau CD and insert the CD into your CD ROM drive. The installation process will start automatically.
- 2. Follow the instructions that appear on your screen.

#### Note

If the installation does not start automatically, you probably have your Windows **Autorun** feature disabled. You will then need to use Windows Explorer and navigate to the CD root directory. Double-click **Autorun.exe**.

#### Seehau Configuration Program

When first started, Seehau loads a configuration file called Startup.bas located in the Macro subdirectory. This file is created by the Seehau Configuration Program and stores Startup.bas in the following default directory created during installation: C:\Nohau\SeehauAVR\Macro

The Seehau software automatically starts Seehau Config if it does not find the startup file.

You do not need to have the emulator connected to the PC to run the Seehau Config Program. However, for the Seehau regular executable to operate properly, you do need the emulator connected with the jumpers properly set.

It is better to get familiar with the emulator in stand-alone mode before connecting to a target hardware system.

#### Connect Tab

To start the Seehau Configuration Program, do the following:

- 1. From the Start menu, select Programs.
- 2. Select Seehau AVR. Then click Config to open the Emulator Configuration dialog box displaying the Connect tab (Figure 9).

Emulator C	figuration
Connect	
1	
-	Emulator Board Address:
2	200 🔽 Use default
3	Select Processor:
5	
4	What is your Trace Type?
	<u>C</u> ancel <u>H</u> elp A <u>b</u> out

Figure 9. Emulator Configuration Dialog Box (Connect Tab)

First select one of the following communication interfaces:

**Emulator Parallel Cable (EPC)**—Communicates with the emulator system through a standard PC parallel port (LPTx).

Low-Cost Industry Standard Architecture Board (LC–ISA)—Communicates with the emulator system through a PC, ISA plug-in board. Includes a cable to connect between the ISA plug-in board and the emulator system.

As an example of setting up your configuration, the LC–ISA communications interface is shown in Figure 9. The EPC communications interface is very similar, and the steps you follow when using the EPC communications interface are almost identical.

The graphical user interface for this dialog box is divided into four regions. Do the following in each region:

- 1. Region 1—Communications Interface: Select either the EPC or LC–ISA communications interface.
- 2. Region 2—Emulator Board Address:

Contains the address of the internal communication link from your computer. For the ISA card, the default address is 200. To use this default, select the **Use default** option.

Emulator Configura	tion			
Hdw Cfg				
понач	Processor CP	U-AVR2313 0	Miscellaneous Mask INT on step Single Step Timer Ext. Reset Enable External Data Ram	
Clock Clock Source: Target/AVR Sour	ce [JP2&3=X] 🗾	POD Cik (KHz): 8000	uP Clock (KHz): 8000	
Reset Delay Mode: Fast Start		V		
	Car	ncel Help	About About	Einish

Figure 10. Emulator Configuration Dialog Box (Hdw Cfg Tab)

3. Region 3—Select Processor:

Click the down arrow and select a CPU type. Select **CPU-AVR8515** if you want to run the time program examples. (See Chapter 7, "Running the Time Program Example.")

4. Region 4—What is your Trace Type?:

Click the down arrow and select **Trace(Yes)**. The trace is a part of the pod so the list defaults to **Trace(yes)**. This pod does not have a **None** option.

5. Click Next. The Hdw Cfg tab opens (Figure 10).

#### Hdw Cfg Tab

Complete the following fields in this tab:

**Processor**—Shows the processor you selected in the **Connect** tab. If the processor listed is incorrect, click **Prev** to return to the **Connect** tab, and select the correct processor.

#### Miscellaneous

- **Mask INT on step**—When selected this option inhibits interrupts during single-stepping. When cleared this option allows single-stepping into an interrupt routine.
- **Single Step Timer**—When selected, this option single steps the timers during emulator singlestepping. This allows cycle-by-cycle debugging of the counter value which is useful for event timing.

Clearing this option enables the timers to continue to count after the program execution is stopped by a user break or breakpoint. Other peripherals, such as SPI, UART, EEPROM, and PORTs, continue to operate when the program execution is stopped. Use this option for cases when stopping the counter while debugging might cause problems, for example, PWM output modes.

• **Ext. Reset Enable**—When selected this option allows the external reset signal on the adapter pin to pass to the AVR when the emulator is running user code through the Go button or from the **Run** menu item, **Reset and Go**.

When cleared, this option enables a reset only through the Seehau user interface.

• External Data Ram—When selected, this option allows the emulator to write to an external data RAM. This is valid only for the 8515/4414 CPUs and is disabled for all others. You can also use the Map Config tab to select whether this external data RAM is contained on the pod or on the target. (See the "Map Config Tab" section later in this chapter.)

**Port Address**—If you are using the LC–ISA for the communications interface, the port address is displayed for reference only. If the port address is incorrect, click **Prev** to return to the **Connect** tab. If you are using the EPC, the port address is ignored and is not available.

**Clock: Clock Source**—From the **Clock Source** field you can select either a pod generated source or a target source for the AVR clock.

- **Target**—When Target source is selected from the drop-down list, an external crystal or clock generator on the target provides the CPU clock and the **uP Clock (KHz)** field is enabled. Use the **uP Clock (KHz)** field to enter a floating point number that represents the clock frequency in KHz. This value will be used for the trace timestamp. (This value is automatically filled in and is informational only when the Pod Source is selected.) Set JP2 and JP3 in the X position.
- **Pod**—When Pod source is selected from the drop-down list, the pod generates the CPU clock in the range of 8000 KHz to 32 KHz. This enables the **POD Clk (KHz)** field where you can select the frequency. Set JP2 and JP3 in the POD position.
- **POD Clk (KHz)**—Pod generated clock speed.
- **uP Clock (KHz)**—Target clock speed.

Reset Delay Mode—(See the following "Setting the Reset Delay Mode" section.)

**Cancel**—Exits without saving the settings for the dialog box.

Help—Displays the Seehau Help file.

**Finish**—Click to save the configuration and exit the dialog box. A window opens asking whether you want to start the emulator. Select **Yes** to launch Seehau. Select **No** to exit Seehau.

#### **Setting the Reset Delay Mode**

Reset delays for the 2313, 4414, 8515, 4434, and 8535 CPUs are:

- Fast start
- Slow start

Reset delays for the 2333 and 4433 CPUs are:

Delay Mode	Delay + Clock Count
0	x + 6 clocks
1	6 clocks
2	xx + 16K clocks
3	x + 6K clocks
4	16K clocks
5	xx + 1K clocks
6	x + 1K clocks
7	1K clocks

#### Reset delays for Tiny12 are

Delay Mode	Delay + Clock Count	Clock Type
0	x + 6K clocks	External Clock
1	6K clocks	External Clock
2	xx + 6K clocks	Internal RC
3	x + 6K clocks	Internal RC
4	6K clocks	Internal RC
5	xx + 6K clocks	External RC
6	x + 6K clocks	External RC
7	6K clocks	External RC
8	xx + 32K clocks	External Crystal
9	xx + 1K clocks	External Crystal
10	xx + 16K clocks	External Resonator
11	x + 16K clocks	External Resonator
12	+ 16K clocks	External Resonator
13	xx + 1K clocks	External Resonator
14	x + 1K clocks	External Resonator
15	+ 1K clocks	External Resonator

- Xx indicates a long delay.
- **x** indicates a medium delay.
- No **x** indicates a shorter delay.

#### **Configuring the Emulator Options From Within Seehau**

From Seehau open the Emulator Configuration window. Select the **Config** menu and click **Emulator**. The **Emulator Configuration** dialog box opens (Figure 11).

There are three tabs across the top of the main **Emulator Configuration** window. When selected, each tab allows you to access the following dialog boxes:

Hdw Cfg:	Set up emulator hardware options.
Map Config:	Map address ranges to the emulator or target
BP Setup	Configure hardware breakpoint ranges.

#### Hdw Cfg Tab

The **Hdw Cfg** tab displays the CPU that is being emulated, displays the port address, sets the clock speed for either Target or Pod sources, sets the reset delay mode and options for single-stepping, external reset signals, and external data RAM.

**Processor**—Displays the processor you selected during the initial configuration. To change this, run Seehau Config. From the **Start** menu, select **Programs**. Then select **Seehau** and click **Config** from the sub menu. The **Connect** tab opens.

Emulator Configurati	on		
Hdw Cfg Map Config	BP Setup		
понац	Processor Pod Address	CPU-AVR2313	Miscellaneous Mask INT on step Single Step Timer Ext. Reset Enable External Data Ram
Clock			
Clock Source:		POD Cik (KHz):	uP Clock (KHz):
Target/AVR Source	e [JP2&3=X]	• 8000 •	8000
Reset Delay Mode: Fast Start			
<u>0</u> K	Apply	<u>Cancel H</u> elp	<u>R</u> efresh

Figure 11. Hdw Config Tab

#### Miscellaneous

- **Mask INT on step**—When selected this option inhibits interrupts during single-stepping. When cleared this option allows single-stepping into an interrupt routine.
- **Single Step Timer**—When selected, this option single steps the timers during emulator singlestepping. This allows cycle-by-cycle debugging of the counter value which is useful for event timing.

Clearing this option enables the timers to continue to count after the program execution is stopped by a user break or breakpoint. Other peripherals, such as SPI, UART, EEPROM, and PORTs, continue to operate when the program execution is stopped. Use this option for cases when stopping the counter while debugging might cause problems, for example, PWM output modes.

• **Ext. Reset Enable**—When selected this option allows the external reset signal on the adapter pin to pass to the AVR when the emulator is running user code through the Go button or from the **Run** menu item, **Reset and Go**.

When cleared, this option enables a reset only through the Seehau user interface.

• External Data Ram—When selected, this option allows the emulator to write to an external data RAM. This is valid only for the 8515/4414 CPUs and is disabled for all others. You can also use the Map Config tab to select whether this external data RAM is contained on the pod or on the target. (See the "Map Config Tab" section later in this chapter.)

**Port Address**—If you are using the LC–ISA for the communications interface, the port address is displayed for reference only. If you are using the EPC, the port address is ignored and is not available. If the port address is incorrect, run Seehau Config. From the **Start** menu, select **Programs**. Then select **Seehau** and click **Config** from the sub menu. The **Connect** tab opens.

**Clock: Clock Source**—From the **Clock Source** field edit you can select either a pod generated source or a target source for the AVR clock.

- **Target**—When Target source is selected from the drop-down list, an external crystal or clock generator on the target provides the CPU clock and the **uP Clock (KHz)** field is enabled. Use the **uP Clock (KHz)** field to enter a floating point number that represents the clock frequency in KHz. This value will be used for the trace timestamp. (This value is automatically filled in and is informational only when the Pod Source is selected.)
- **Pod**—When Pod source is selected from the drop-down list, the pod generates the CPU clock in the range of 8000 KHz to 32 KHz. This enables the **POD Clk (KHz)** field where you can select the frequency. Set JP2 and JP3 in the POD position.
- **POD Clk (KHz)**—Pod generated clock speed.
- **uP Clock (KHz)**—Target clock speed.

Reset Delay Mode—(See the preceding "Setting the Reset Delay Mode" section.)

**OK**—Saves the settings for this tab and exits the dialog box.

Apply—Saves the settings for this tab.

Cancel—Exits without saving the settings for the dialog box.

Help—Displays the Seehau Help file.

Refresh—Allows you to retrieve and view the current emulator hardware configuration settings.

#### Map Config Tab

CPUs with external data memory have the option of using the on-pod 64K data RAM or external target RAM. Normally, the pod defaults to using the on-pod RAM.

External target RAM can be selected by mapping the RAM to the target. This is accomplished by setting up an address range in the Map Config tab that will select the target RAM. Separate blocks of RAM can be selected for mapping to the target. The granularity of the mapping addresses is 256 bytes per block. The first valid block is at 0x300 through 0x3FF.

Multiple blocks can be mapped to the target with one range selection. For example, the range 0x300:0xFFFF would select all blocks for the target.

Emulator Configuration	
Hdw Cfg Map Config BP Setup	
Map to Target Memory	
✓         0x0700:0x7FF           ✓         0x1000:0x1FFF           ✓         0x3000:0x30FF	Add Edit Remove
<u>QK</u> <u>Apply</u> <u>Cancel H</u> elp <u>R</u> efresh	

Figure 12. Map Config Tab

Map to Target Memory display area—Displays the address ranges that are mapped to the target.

**Add**—Opens the **Add Address Range** dialog box. Entries can be done with hex address or symbolically.

Edit—Select an address range in the Map to Target Memory display area, then click Edit. The Add Address Range dialog box opens. Make any changes to the values, then click OK.

**Remove**—To remove an address range, select the address range in the **Map to Target Memory** display area, then click **Remove**.

**Remove All**—Removes all displayed address ranges.

**OK**—Saves the settings for this tab and exits the dialog box.

Apply—Saves the settings for this tab.

Cancel—Exits without saving the settings for the dialog box.

Help—Displays the Seehau Help file.

Refresh—Allows you to retrieve and view the current emulator hardware configuration settings.

#### **BP Setup Tab**

The **BP Setup** tab configures hardware breakpoint ranges.

**Hardware Breakpoints** display area—Displays the address ranges that are enabled for hardware breakpoints.

Emulator Configuration	
Hdw Cfg Map Config BP Setup	
Hardware Breakpoints	
	Add Edit Bernove Remove All
<u>QK</u> <u>Apply</u> <u>Cancel H</u> elp <u>R</u> efresh	

Figure 13. BP Setup Tab

Add—Opens the Add Address Range dialog box. Entries can be done with hex address or symbolically.

Edit—Select an address range in the Hardware Breakpoints display area, then click Edit. The Add Address Range dialog box opens. Make any changes to the values, then click OK.

**Remove**—To remove an address range, select the address range in the **Hardware Breakpoints** display area, then click **Remove**.

**Remove All**—Removes all displayed address ranges.

**OK**—Saves the settings for the tabs and exits the dialog box.

Apply—Saves the settings for this tab.

Cancel—Exits without saving the settings for the BP Setup dialog box.

Help—Displays the Seehau Help file.

Refresh—Allows you to retrieve and view the current emulator hardware configuration settings.

#### Add Address Range Dialog Box

Begin address—Enter the first address of the range.

**End address**—Enter the last address of the range.

**OK**—Saves the settings for the tabs and exits the dialog box.

Cancel—Exits without saving the settings for the Add Address Range dialog box.

Help—Displays the Seehau Help file.



Figure 14. Add Address Range Dialog Box



Always power up the emulator before applying power to the target. Always turn off the target power before turning off the emulator power. Power flowing from the target into the emulator can damage it. Connect the ground wire before connecting the emulator processor pins to the target.

If it is necessary to separate the adapter from the emulator board, use extreme care. Only minimal force is necessary to separate the connectors. Excessive force can tear the connectors from the board. This cannot be repaired and is not covered under warranty. See Nohau's Web site for further information: <u>http://www.nohau.com/techpub/adaptdisc2.pdf</u>
# **5** Introduction to Tracing

## **Overview of Tracing**

The trace feature provides the same basic capabilities as a logic analyzer. Each trace frame is time stamped and records the following fields: address and data values, cycle type, I/O ports, and up to eight external inputs.

By default, trace automatically starts recording when you begin user code execution. When you stop code execution, the trace history is displayed automatically. You can set up trigger and/or filter conditions to control the trace recording. (See Chapter 6, "Configuring Trace Triggers.")

Tracing allows you to perform many tasks, including:

- Detecting an error condition
- Analyzing a history of the sequence of events leading to an error
- Sampling time measurements
- Analyzing peripheral I/O
- Characterizing code behavior using tools such as Program Performance Analysis (PPA) and Code Coverage (available only with Enhanced Trace)

The Seehau provides an interface for the trace setup display.

## **Trace Features**

- Records and qualifies addresses for filtering and triggering.
- Records up to eight miscellaneous signals in addition to the address, data, and control signals.
- Records 36 bits of timestamp information at full resolution down to 125 nanoseconds. This allows the timestamp counter to run for more than two hours without overflowing.
- Continues to run the user program without interruption while the trace stops, is reconfigured, and starts again as many times as required.

### **Trace Display Window**

You can open a Trace window by doing one of the following:

- From the **New** menu, select **Trace**.
- Click the New Trace Window icon (TR) in the toolbar.

🔛 Trac	Trace_1							
Frame								
-16	timer.hour=10;							
-11	timer.min=17;							
-6	timer.sec=10;							
-1	<pre>strcpy(timer.am_pm,"pm");</pre>							
4								
SOURCE	ONLY got frames Frames:17(-16:0), Trig Count:0							

Figure 15. Source Only Displays Executed Source Lines

Tra	ce_1										- D ×
Frame	Abs.	time	Addres	s Opcode	Instr.		Symbol	Status	XAddr:XData	Ports C A D B	<b>_</b>
-15	timer.	hour=	=10;								
-15	306.62	25 us	008	4 E00A	LDI	R16, OxA				{05 1C C0 00}	
-14	306.75	iO us	008	3 93000552	STS	timer, R16				{05 1C C0 00}	
-10	timer.	min=1	L7;								
-10	307.25	iO us	008	) E101	LDI	R16, 0×11		{wr}	****:OA	{05 0A 80 00}	
-9	307.37	'5 us	008	5 93000553	STS	0x553, R16				{05 52 C0 00}	
-5	timer.	sec=:	LO;								
-5	307.87	'5 us	009	) E00A	LDI	R16, O×A		{wr}	****:11	{05 11 80 00}	
-4	308.00	)0 us	009	L 93000554	STS	0×554, R16				{05 53 C0 00}	
U	strcpy	(time	er.am_p	n,"pm");							
0	308.50	)0 us	009	3 E947	LDI	R2O, O×97		{wr}	****:OA	{05 0A 80 00}	
1	308.62	25 us	009	4 E055	LDI	R21, 0×5				{05 54 C0 00}	
	_										±
<u> </u>											<u> </u>
MIXED	got fram	es  Fran	nes:17(-15	:1), Trig Count	0						11.



Tra	ce_1										
Frame	Rel. t	ime Address	Opcode	Instr.		Symbol	Status	XAddr:XData	Ports C	ADB	L 🔄
-15	0 ns	008A	EOOA	LDI	R16, OxA				{05 1C	CO 00}	
-14	125 ns	008B	93000552	STS	timer, Ri	L6			{05 1C	CO 00}	
-13	125 ns	008C	0552				{fetch}		{05 1C	CO 00}	
-12	125 ns	008D					{Xaddr}	0552:**	{05 52	CO 00}	
-11	125 ns	008D					{XData}	****:OA	{05 0A	80 00}	
-10	125 ns	008D	E101	LDI	R16, 0×11	L	{wr}	****:OA	{05 0A	80 00}	
-9	125 ns	008E	93000553	STS	0×553, R1	16			{05 52	CO 00}	
-8	125 ns	008F	0553				{fetch}		{05 52	CO 00}	
-7	125 ns	0090					{Xaddr}	0553:**	{05 53	CO 00}	
-6	125 ns	0090					{XData}	****:11	{05 11	80 00}	
-5	125 ns	0090	EOOA	LDI	R16, OxA		{wr}	****:11	{05 11	80 00}	
-4	125 ns	0091	93000554	STS	0×554, R1	16			{05 53	CO[00}	
-3	125 ns	0092	0554				{fetch}		{05 53	CO 00}	
-2	125 ns	0093					{Xaddr}	0554:**	{05 54	CO 00}	
-1	125 ns	0093					{XData}	****:OA	{05 0A	80 00}	
0	125 ns	0093	E947	LDI	R20, 0×97	?	{wr}	****:OA	{05 0A	80 00}	-
1	125 ns	0094	E055	LDI	R21, 0×5				{05 54	CO 00}	±
•											<u>▶</u> ∓
TRACE	ONLY got	t frames Frames	:17(-15:1), Tri	g Count:0							

Figure 17. Trace Only and Non-Compressed Displays Assembly Code for Each Cycle

#### **Trace Window Columns**

**Frame Number**—Frame 0 represent the trigger frame. Earlier frames have negative numbers. Post-trigger frames have positive numbers. If there is no trigger, Frame -1 is the last frame in the buffer.

**Time Stamp**—Displays one of the following formats based on selections in the **Trace Display** options local menu:

- **Relative Time**—Amount of elapsed time since the beginning of the previous instruction.
- Absolute Time—Amount of elapsed time since the last GO or trace restart.
- **Relative Cycle**—Number of CPU cycles since the beginning of the previous instruction.
- Absolute Cycle—Number of CPU cycles since the last GO or trace restart.

Address—Address of instructions.

**Opcode**—Hexadecimal instruction display.

Instruction—Assembly instruction mnemonics.

Symbol—Symbolic label for an instruction address from the compiler.

Status—Display of the current cycle type

- Blank—Start of executing instruction
- {**fetch**}—An un-executed instruction or command is fetching an address or look-up table data from code memory.
- {wr}—Write strobe to external RAM
- {rd}—Read strobe to external RAM
- {Xaddr}—External RAM address is present on Port C and Port A.
- {Xdata}—External RAM Read or Write data is present on Port A when you select one wait state.

Xaddr:Xdata—Decoded version of the multiplexed interface to the external RAM.

- 0553:\*\*—Address 0553 found on Port C and Port A.
- \*\*\*\*:**1B**—Data 1B found on Port A during rd or wr strobe.

**Ports C, A, D, and B**—(port data) This order groups the external RAM interface signals together. Note that four ports are always shown, even if they do not exist for a given CPU.

**{05** | **1B** | **40** | **00**}—Port C = 05, Port A = 1B, Port D = 40, and Port B = 00 (hex).

Misc—Displays the eight inputs from the Trace Misc Inputs connector.

	<u>G</u> o to Frame number Find <u>T</u> rigger Point ⊇ero Time at Cursor Synchronize Source Window <u>D</u> isplay mode	Shift+Ctrl+F Ctrl+Z
	<u>Find</u> Find Ne <u>x</u> t Find Pre <u>v</u> ious Show So <u>u</u> rce Line Fi <u>l</u> e	Ctrl+F F3 Alt+F3
********	Show TimeStamp <u>Belative TimeStamp</u> <u>Convert Cycles to Time</u> Show <u>Misc. Data</u> Show External <u>B</u> us Show Ports Show Opcode Show Status Show Symbol Compressed <u>All Options</u>	
	Trac <u>e</u> Config Settjngs Cha <u>ng</u> e Caption	•

Figure 18. Local Trace Menu

#### Trace Menu

To access the **Local Trace** menu, right click the Trace window or select the **Trace** menu which appears in the main menu bar only when the Trace window is active (Figure 18).

**Go to Frame number**—Opens a dialog box where you can enter a specific frame number for display.

Find Trigger Point—Displays the trigger point (frame zero).

**Zero Time at Cursor**—Changes the timestamp at the selected frame to zero and makes all other timestamps relative to the selected frame.

**Synchronize Source Window**—Automatically aligns the display of code in the Source window as you scroll through the Assembly code in the trace buffer.

**Display mode**—Opens a submenu that allows you to select which code to display:

- Trace Only—Displays Assembly code only in the trace buffer.
- Mixed (Trace and Source)—Displays both C and Assembly code in the trace buffer.
- **Source**—Displays C source code only in the trace buffer.

Find—Not implemented.

Find Next—Not implemented.

Find Previous—Not implemented.

**Show Source Line**—Displays the associated source code for the current frame. The frame address must match a source line address.

Save Trace To File	×
Frame Range         C All(-74:2)         • Current Window(-7:2)         C Frames Erom       0000         Io       0000	Mode Mixed(Trace and Sou
File (C:\NOHAU\SEEHAUAVR\macro) File Name	<u>B</u> rowse
<u>O</u> k Cancel <u>H</u> elp	

Figure 19. Save Trace To File Dialog Box

#### File

- Save to File—Opens the Save Trace To File dialog box where you can save the contents of the trace buffer as text to a file (Figure 19). In the Frame Range group select one of the following:
  - All: Saves the entire trace buffer.
  - Current Window: Saves only the contents of the current Trace window.
  - Frames: Allows you to specify a range of frames.
- **Print**—Allows you to send the trace buffer to a printer.

#### Note

The following menu items can be toggled individually or can be configured all at once. Click **All Options** to open the **Display Options** dialog box.

**Show TimeStamp**—Displays the timestamp which represents the number of machine cycles that have elapsed since the beginning of program execution.

**Relative TimeStamp**—Displays the timestamp as the number of machine cycles that have elapsed since the execution of the previous instruction.

**Convert Cycles to Time**—Converts the timestamp from machine cycles to actual time based on the microprocessor clock (uP clock).

Show Misc. Data—Displays eight inputs from the Misc Trace Inputs connector.

**Show External Bus**—Displays a decoded version of the multiplexed address/data bus going to the external data RAM.

Show Ports—Displays the CPU I/O ports. (Displayed ports are not valid for all CPUs.)

Show Opcode—Displays the hexadecimal instruction.

Show Status—Displays bus cycle type (Fetch, Write, or Read).

Show Symbol—Displays symbolic labels associated with the address field.

Compressed—Displays executed code only. (Note: Not all RD/WR cycles are shown.)

**All Options**—Opens the Display Options window where you can select or clear trace options in a single update.

**Trace Config**—Opens the **Trace Configuration** dialog box. Refer to Chapter 6, "Configuring the Trace" in this guide.

Settings—Opens a submenu that allows you to set up Trace window attributes.

Change Caption—Allows you to change the Trace window caption in the title bar.

# **6** Configuring Trace Triggers

Trace Configuration	
Trace Setup	
Enable Trace Window Mode	🗖 Enable Trigger
Start Trace Condition	Trigger Condition
Instruction Start     timer1_isr	Address
External Data Read	🗖 External Data Read
External Data Write	External Data Write timer.sec
Pause Trace Condition Address	Post Trigger Count 3
✓ Instruction Start timer1_isr_END	
🗖 External Data Read	🗖 Break on Trace Stop
🗖 External Data Write	
<u>QK</u> <u>Apply</u> <u>Cancel</u> <u>H</u> elp	<u>R</u> efresh

Figure 20. Trace Setup Tab

Trace recording can be started and stopped automatically by defined conditions that you set. This reduces the clutter in the trace display by only recording the cycles that you specify.

To open the **Trace Setup** tab from the **Config** menu, select **Trace**. The **Trace Setup** tab opens (Figure 20).

Selecting the **Enable Trace Window Mode** option enables the trace recording to start and pause. The Window mode will start trace recording on a selected **Start Trace Condition**, and pause trace recording on a selected **Pause Trace Condition**.

Selecting the **Enable Trigger** option enables the trace to be controlled by a trigger. The trigger will cause the trace to start recording and continue until the **Post Trigger Count** has reached zero. At that time, trace recording stops, and you can view the results in the Trace display window.

The trigger can be used with or without the Window mode. If the Window mode is not used and the trigger is enabled, the trace will start recording as soon as you click the Go button to start emulation. The trigger will, when encountered, perform the decrement of the **Post Count** to zero and then stop the trace and display the results Trace display window.

The following trace conditions cause a trace start, pause, or trigger:

- Instruction Start—Executed Instruction Start Addresses
- External Data Read—External Data RAM Read Addresses
- External Data Write—External Data RAM Write Addresses

The values entered in these fields can be numerical addresses or compiler source symbols for either the code address or the symbols for external RAM data variables.

All three of the types of trace conditions can be present and operate in parallel, that is, the conditions are logically ORd.

The **Post Trigger Count** indicates the number of CPU cycles that continue after a trigger. Tracing stops at the end of the post trigger count.

Select the **Break on Trace Stop** option to stop running user code when tracing has stopped from the final post trigger count.

**OK**—Saves the settings for this tab and exits the dialog box.

Apply—Saves the settings for this tab.

Cancel—Exits without saving the settings for the Trace Setup tab.

Help—Opens the Seehau Help file.

**Refresh**—Allows you to retrieve and view the current trace and emulator hardware configuration settings.

# **Z** Running the Time Program Example

## **Getting Started**

The Time\_AVR8515.d90 example program is located in the C:\Nohau\SeehauAVR\Examples directory.

- **1.** To set the processor type, refer to Chapter 4, "Installing and Configuring the Seehau Software."
- 2. Set the Processor to AVR8515 and select the External Ram option. Click Finish to start Seehau. (Figure 21).

To load the example program and configure the Seehau display, do the following:

- 1. From the Config menu select Load Settings. The Open dialog box opens.
- 2. Select Timer\_window.bas from the Macro directory. Then click Open.

The Time\_AVR8515 example program uses timer 1 to generate a one millisecond interrupt which is then counted. When 1000 milliseconds have elapsed, the time.sec value changes and the time display in the Shadow Data window is updated.

Emulator Configu	ration			
Hdw Cfg				
понац	Processor	CPU-AVR8515	Miscellaneous Mask INT on step Single Step Timer Ext. Reset Enable Katernal Data Ram	
Clock Clock Source: Pod Source [JF	P2&3= Pod]	POD Clk (KHz):	uP Clock (KHz): 8000	
Reset Delay Mode	3:	×		-
		<u>C</u> ancel <u>H</u> elp	About 🔶 Prev	<u>F</u> inish

Figure 21. Hdw Cfg Tab Set for Running the Time Program Example

## **Setting the Trace Window Mode**

The Timer\_window.bas macro has automatically set up the trace Window mode to record instructions only when the timer interrupt routine is active.

To manually set up the trace Window mode, do the following:

- 1. From the Config menu select Trace. This opens the Trace Setup tab (Figure 20).
- 2. Select the Enable Trace Window Mode option.
- **3.** In the Start Trace Condition group select the **Instruction Start** option and enter the start symbol timer1\_isr in the **Address** text field.
- 4. In the Pause Trace Condition group select the **Instruction Start** option and enter the start symbol timer1\_isr\_END in the **Address** text field. (There are two underscore characters before END.) Your **Trace Setup** tab should look like Figure 20.
- 5. Click **OK** to save your trace configuration.
- 6. Click the Go button on the toolbar to start the program. The Trace button turns red indicating the trace is active. You can stop the trace by clicking the TR or STOP buttons. The Trace window will display the latest trace record.
- Set the Trace window display mode by right-clicking within the data area of the Trace window. This opens the local Trace menu. Select Display Mode and then click Source Only. Your Trace window will look like Figure 22. Note that the interrupt routine occurs repeatedly.



Figure 22. Trace\_1 Window Displaying Source Only

## **Trace Triggers**

#### Adding a Trace Trigger

You can add a trigger condition to automatically stop the trace recording by doing the following:

- 1. From the **Config** menu select **Trace** to open the Trace Configuration window displaying the **Trace Setup** tab.
- 2. Select the Enable Trigger option.
- **3.** In the Trigger Condition group select the **External Data Write** option and enter the data symbol name Timer.sec in the **Address** text field.
- 4. Set the Post Trigger Count to 3.
- 5. Click **OK** to save your trace configuration.
- 6. Click the Go button on the toolbar to start the program. The Trace button turns red and then green indicating the trace has stopped recording.

The last frame number under the Frame column is positive indicating a trigger has occurred. The last interrupt routine displays a different line at frame –8 indicating a write to Timer.sec has occurred. This is the trigger condition.



Figure 23. Trace Trigger in Source Only Mode

#### **Changing the Trace Display Mode**

To change the trace display mode do the following:

- 1. Right-click within the data area of the Trace window. This opens the local Trace menu. Select Mixed (Trace and Source).
- 2. Right-click again within the data area and select **Compressed**. Your Trace\_1 window should look like Figure 24.

The source line of the trigger event is displayed at Frame -8 (timer.sec++;). The assembly code is displayed at Frames -8, -4, and -3. Frame -3 displays the assembly instruction STS 0x554, R16. This is the trigger instruction.

#### Viewing the Trigger Cycle

To view the trigger cycle do the following:

- 1. Right-click within the data area of the Trace window. This opens the local **Trace** menu. Select **Trace Only**.
- **2.** Right-click again within the data area and select **Non-Compressed**. Your Trace\_1 window should look like Figure 25.

Trace_	1														_ 🗆	×
Frame	Rel. t	ime Ad	ldress	Opcode	Instr.			Symbol		Status	XAddr:XData	Ports	сa	DВ	Misc.	
-29	if (ti	cks ==	1000)										_			1
-29	500 ns	:	0067	91000520	LDS	R16, ti	cks			(wr)	****:03	{05 03	80	100}	FF	
-25	500 ns	1	0069	91100521	LDS	R17, Ox	:521			{rd}	****:E8	(05 E8	40	100}	FF	
-21	500 ns	(	006B	3208	CPI	R16, 0x	E8			(rd)	****:03	{05 03	40	100}	FF	
-20	125 ns	1	006C	4013	SBCI	R17, Ox	:3					{05 21	CO	100}	FF	
-19	125 ns	1	006D	F459	BRNE	20011						{05 21	00	100}	FF	
-18	ticks	= 0;														
-18	125 ns	(	0068	2700	EOR	R16, R1	.6	==> ?00	10:			{05 21	CO	100}	FF	
-17	125 ns	1	006F	2711	EOR	R17, R1	.7					(05 21	CO	100}	FF	
-16	125 ns	1	0070	93000520	STS	ticks,	R16					(05 21	CO	100}	FF	
-12	500 ns	1	0072	93100521	STS	0x521,	R17			(wr)	****:00	{05 00	80	(00)	FF	
-8	timer.	sec++;														
-8	500 ns	t.	0074	91000554	LDS	R16, Ox	:554			(wr)	****:00	{05 00	80	100}	FF	
-4	500 ns	1	0076	SFOF	SUBI	R16, ?0	022			(rd)	****:OD	(05 0D	40	(00)	FF	
-3	125 ns	1	0077	93000554	STS	0x554,	R16					{05 54	CO	(00)	FF	
1	}															
1	500 ns		0079	9009	LD	RO, Y+		==> ?00	11:	{wr}	****:OE	(05 0 <b>E</b>	80	100}	FF	⊡
	_															*
<u> </u>													_		•	1-
MIXED got I	frames Fr	rames:541	110(-541	07:2), Trig Co	bunt:0											11

Figure 24. Trace Display in Mixed (Trace and Source) Mode

Trace_	1												- 🗆	×
Frame	Rel. time	Address	Opcode	Instr.		Symb	01	Status	XAddr:XData	Ports	C A	D B	Misc	
-14	125 ns	0072						{Xaddr}	0520:**	{05 20	[C0]	00}	FF	1
-13	125 ns	0072						(XData)	****:00	{05 00	80	00}	FF	
-12	125 ns	0072	93100521	STS	0x521, R	17		(wr)	****:00	{05 00	1801	00}	FF	
-11	125 ns	0073	0521					{fetch}		{05 20	C O	00}	FF	
-10	125 ns	0074						{Xaddr}	0521:**	{05 21	1001	00}	FF	
-9	125 ns	0074						(XData)	****:00	{05 00	1801	00}	FF	
-8	125 ns	0074	91000554	LDS	R16, 0x53	54		(wr)	****:00	{05 00	801	00}	FF	
-7	125 ns	0075	0554					{fetch}		{05 21	1001	00}	FF	
-6	125 ns	0076						{Xaddr}	0554:**	{05 54	1001	00}	FF	
-5	125 ns	0076						{XData}	****:OD	{05 0D	40	00}	FF	
-4	125 ns	0076	SFOF	SUBI	R16, 2002	22		(rd)	****:0D	{05 0D	40	00}	FF	
-3	125 ns	0077	93000554	STS	0x554, R	16				{05 54	1001	00}	FF	
-2	125 ns	0078	0554					{fetch}		{05 54	1001	00}	FF	
-1	125 ns	0079						{Xaddr}	0554:**	{05 54	1001	00}	FF	
0	125 ns	0079						{XData}	****:OE	(05 0E	801	00}	FF	
1	125 ns	0079	9009	LD	RO, Y+	= $=$ $>$	?0011:	{wr}	****:OE	{05 0E	801	00}	FF	
2	125 ns	007A	BEOF					{fetch}		{05 54	1001	00}	FF	-
•													Þ	Ŧ
TRACE ONL	Y got frames	Frames:829	94(-82991:2),	Trig Count:0										//

Figure 25. Trace Display in Trace Only Mode

Frame 0, where the trigger cycle occurred, shows a status of **{XData}**. This indicates the first cycle of a 1-wait state read/write cycle. The next line, Frame 1, indicates a status of **{wr}** indicating a final write cycle. Frame –1 is where the multiplexed address/data bus was driving the address **Xaddr:XData = 0554:\*\***. Address 0554 is timer.sec, the address of the trigger condition.





Figure 26. Atmel 3100 Adapter

## Overview

The connection from the emulator to the target is made through an adapter that fits on the bottom of the POD–AVR. There are five adapters that cover the eight CPU DIP pinouts:

CPU	Atmel Adapter
8515/4414	3000
8535/4434	3100
2333/4433	3200
2313	3300
Tiny12	3400

## **Tiny12 Oscillator Options**

The Tiny12 CPU has special oscillator pin options that are implemented with zero-Ohm resistor jumpers on the 3400 adapter. Selecting these options requires resoldering the resistors.

Oscillator Type	Oscillator Source	Pin 2 Function	Pin 3 Function	Zero-Ohm Jumper Location	
				PB3 : XTAL1	PB4 : XTAL2
Internal RC	Internal	PB3 I/O	PB4 I/O	—— : Open	: Open
External clock to Xtal1 (or ext. RC)	Target	XTAL1	PB4 I/O	Open: ——	: Open
Crystal or resonator	Target	XTAL1	XTAL2	Open: ——	Open: ——
Crystal or resonator	Adapter	None	None	: Open	: Open
Pod clock *	EMUL-AVR	None	PB4 I/O	: Open	: Open

#### Note

------ indicates the installed zero-Ohm resistor jumper position.

\* To use the pod clock, set JP2 and JP3 to the Pod position. For all other oscillator options, set JP2 and JP3 to the X position.

## **Adapter Mounted Crystals**

The 3300 adapter for the AVR2313 and the 3400 adapter for the Tiny12 provide a mounting area for a crystal. There are land patterns for the SMD capacitors from the crystal legs to the ground. The 3300 adapter crystal is wired directly to the target-side pins. The 3400 adapter allows you the option of connecting the adapter-mounted crystal to the target or not. (Refer to the previous table.)

# **9** Troubleshooting

## **Check List**

Before you start troubleshooting, first check the following items:

- Are the cables connected properly?
- If the pod is connected through the LC/ISA, is the EPC power jumper removed?
- If the pod is connected through the EPC, is the EPC power jumper installed?
- Did you configure Seehau correctly for your MCU?
- If the pod is not connected to your target, are the power and crystal jumpers in the Pod position?
- If the pod is connected to your target, is the target power turned on?

## EPC

While starting the emulator, look at the Logic and Reset LEDs.

#### Step 1. Does the Reset LED flash and then remain off?

- Yes. Go to Step 2.
- No. Go to Step 3.

#### Step 2. Does the Logic LED turn from red to green?

- Yes. Go to Step 4.
- No. Go to Step 3.

## Step 3. Does the LPT port match the values in the Seehau configuration?

- **Yes**. The LPT port matches the values:
  - 1. From the **Start** menu, select **Programs**.
  - 2. Select Windows Explorer or NT Explorer and go to the directory where you installed the SeehauAVR software and open the Macro sub-directory.

- 3. Open the Startup.bas file in a text editor. Look for lines similar to the following: Cfg\_ConnectionType "LPT1:"
- 4. The values set here should match the correct LPT port in the computer.

If you still encounter problems, contact Nohau Technical Support.

• **No**. The LPT port does not match the values.

Enter the correct LPT port value that matches the computer's LPT port that the EPC is connected to.

If you still encounter problems, contact Nohau Technical Support.

#### Step 4. Yes the LEDs operate correctly. Does Seehau start

- **Yes**. Troubleshooting is complete!.
- **No**. Seehau does not start. The Reset LED flashed, but the Logic LED remains red.
  - Re-install the software and try again (in case of a bad copy of the logic file).
  - Refer to the "Debugging the Parallel Port" section.
- **No**. The Reset LED does not flash. Contact Nohau Technical Support.

## **Debugging the Parallel Port**

**Step 1**. Disconnect other devices that might be sharing this parallel port (such as printers, zip, or jazz drives, parallel CD ROM drives, or software dongle keys).

Now is it working?

- **Yes**. You're done. You might opt to purchase an additional parallel port card.
- **No**. Do the following:

#### **NT Users**

Check the NohauAVR driver status by doing the following:

- To check the status, go to the Start menu. Select Control Panel. Then double-click Devices.
  - If the status shows **Started**, go to **Step 2**.
  - If the status shows **Stopped**, check the ParPort driver for **Started** status.
  - If the ParPort driver shows **Stopped** click **Start**.
- Now re-check the driver status.
  - If the driver shows **Started**, try restarting Seehau.
  - If the ParPort driver still shows **Stopped**, go to NT Diagnostics:
    - 1. From the Start menu, select Programs.
    - 2. Then select **Administrative Tools**, and click **Windows NT Diagnostics**. The Windows NT Diagnostics window opens.
    - 3. Click the **Resources** tab.
    - 4. Click **I/O Port**. Scroll down to address 378 (LPT1) and look for a device at this address.
    - 5. From the Control Panel, double-click **Devices**. Disable the device located at 378.
    - 6. Attempt to restart Seehau. If this fails, go to **Step 2**.

#### Windows 9x Users

Check the parallel port mode. Go to **Step 2**.

#### Windows 2000 Users

Verify that the NohauAVR device driver is properly installed. Do the following:

- 1. From the Start menu, select Programs. Select Accessories, then click System Tools.
- 2. Double-click System Information. The System Information window opens (Figure 27).

System Information		
Action View Tools +	>   🖻 📧   🗗 🎒 🚺	5 😫   🖬 🛎 🗊 🔕
Tree	Item	Value
System Information System Summary Hardware Resources Components Software Environment Turnet Explorer 5	Item OS Name Version OS Manufacturer System Name System Manufacturer System Model System Type Processor BIOS Version Windows Directory Locale Time Zone Total Physical Memory Ouvilable Dusciral Memory	Value         Microsoft Windows 2000 Professional         5.0.2195 Build 2195         Microsoft Corporation         FTL         Not Available         Not Available         X86 Family 6 Model 5 Stepping 1 GenuineIntel ~400         PhoenixEIOS 4.0 Release 6.0         D:\WINNT         United States         Pacific Daylight Time         130,604 KB
	Available Physical Memory Total Virtual Memory Available Virtual Memory Page File Space	43,040 KB 442,056 KB 267,704 KB 311,452 KB

Figure 27. System Information Window

- 3. Click Software Environment.
- **4.** Click **Drivers** to display a list of active drivers. Refer to the **Name** column and scroll down to NohauAVR (Figure 28).
- 5. In the State column, verify the driver is running. In the Status column, you should see OK.

🔝 System Information						<u>_   ×</u>
🛛 Action Yiew Tools 🗍 年	→   🗈 💽	e 4 d B   2   5	] 🖻 🗊 🔕			
Tree	Name	Description	Туре	State	Status	<b>_</b>
<ul> <li>System Information</li> <li>System Summary</li> <li>Hardware Resources</li> <li>Components</li> <li>Software Environment</li> <li>Environment Variables</li> <li>Jobs</li> <li>Network Connections</li> <li>Running Tasks</li> <li>Loaded Modules</li> <li>Services</li> <li>Program Groups</li> <li>Startup Programs</li> <li>OLE Registration</li> <li>Internet Explorer 5</li> </ul>	nohau51 nohau47 nohau47 nohau47 nohau5	NohauS1 NohauS1 NohauAVR NohauAX Nohau_XA Npfs NI Apm/Legacy Interface Ntfs Null IPX Traffic Filter Driver IPX Traffic Filter Driver Parallel class driver Parallel port driver Parallel port driver Parallel port driver PartNgr PCI Bus Driver PCI Bus Driver PCI Dump PCI Bus Driver PCIDump PCIIde Pemcia perm2 WAN Miniport (PPTP) Direct Parallel Link Driver ql1080 Ql10wnt	Kernel Driver Kernel Driver Kernel Driver Kernel Driver Kernel Driver File System Driver File System Driver Kernel Driver	Running Running Running Running Running Stopped Stopped Stopped Running Running Running Running Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped Stopped	OK           OK	

Figure 28. List of Active Drivers

System Properties	? ×
General Network Identification Hardware User Profiles Adv	vanced
Hardware Wizard The Hardware wizard helps you install, uninstall, repu unplug, eject, and configure your hardware.	air,
Hardware Wize	ard
Device Manager	
The Device Manager lists all the hardware devices i on your computer. Use the Device Manager to chan properties of any device.	nstalled ge the
Driver Signing Device Manag	jer
Hardware Profiles	
Hardware profiles provide a way for you to set up an different hardware configurations.	d store
Hardware <u>P</u> rofi	les
OK Cancel	Apply

Figure 29. System Properties Window

If the ParPort driver still shows "Stopped," do the following:

- 1. Right-click the My Computer icon on your desktop, and select **Properties**. The System Properties window opens (Figure 29).
- 2. Click the Hardware tab. Then click Device Manager. The Device Manager window opens (Figure 30).



Figure 30. Device Manager Window

🖳 Device Manager
J Action View J ← →   🛍 🖬 😫 J 🗟
E- 🖳 FTL
🗄 🛄 Direct memory access (DMA)
🖃 🛄 Input/output (IO)
[00000000 - 0000000F] Direct memory access controller
[00000064 - 00000064] PC/AT Enhanced PS/2 Keyboard (101/102-Key)
[00000081 - 0000008F] Direct memory access controller
[00000090 - 00000091] PCI bus
[00000093 - 0000009F] PCI bus
[000000A0 - 000000A1] Programmable interrupt controller
CONTRACT - CONTRACT Direct memory access controller
[00000100 - 00000CP7] PCI Dus [00000120 - 00000127] Crustal WDM Audia Castral Desisters
[00000120 - 00000127] Crystal WDM Audio Control Registers     [00000170 - 00000127] Secondary IDE Chappel
[00000220 - 00000233] Clystal work Addio Codec
[00000274 - 00000277] ISAPNP Read Data Port
[00000279 00000279] ISAFNA Kead Bata Fort
100000330 - 000003311 Crystal WDM MPL-401 Compatible
[00000370 - 00000371] Motherboard resources
[00000380 - 00000388] Diamond Multimedia Fire GL1000 Pro

Figure 31. Device Manager Window Displaying the System Resources

- **3.** In the Device Manager window, select the **View** menu. Then click **Resources by Type**. A window appears that shows the system resources (Figure 31).
- 4. Double-click Input/Output (I/O).
- Scroll down to address 378 (LPT1) and look for a device at this address. Go back to the Control Panel and double-click **Devices**. Disable the device located at address 378. Attempt to restart Seehau. If this fails, proceed to **Step 2**.

**Step 2.** Check the parallel port mode.

- 1. Reboot and enter BIOS setup. From BIOS setup, check for one of the following parallel port modes:
  - Normal
  - Standard
  - Compatible
  - Output only
  - Bi-directional
- 2. Ensure that one of these modes is selected.
- **3.** Then try selecting another mode.
- 4. Save your settings and reboot.

#### Note

The following modes have been known to cause problems: ECP, EPP, or ECP + EPP.

## ISA

While starting the emulator, look at the Logic and Reset LEDs.

#### Step 1. Does the Reset LED flash and then remain off

- Yes. Go to Step 2.
- No. Go to Step 3.

#### Step 2. Does the Logic LED turn from red to green

- **Yes**. Go to **Step 4**.
- No. Go to Step 3.

## Step 3. Do board I/O addresses match the values in the Seehau configuration?

- **Yes**. The I/O addresses match the values:
  - 1. From the **Start** menu, select **Programs**.
  - 2. Select Windows Explorer or NT Explorer and go to the directory where you installed the SeehauAVR software and open the Macro sub-directory.
  - Open the Startup.bas file in a text editor. Look for lines similar to the following: Cfg\_EmulBoardAddr "200" Trace\_TraceBoard "Trace(yes)" Trace\_TraceBoardAddr "200"
  - 4. The values set here should match the hex value that is set on the ISA communication board. Refer to the Installing the ISA Plug-In Board. . ." sections in Chapter 2, "Installing and Configuring the Communications Interface."

If you still encounter problems, contact Nohau Technical Support.

• **No**. The I/O addresses do not match the values.

Enter the correct hex value in both locations that match the ISA board's address.

#### Step 4. Yes the LEDs operate correctly. Does Seehau start

- **Yes**. Troubleshooting is complete!.
- No. Seehau does not start. The Reset LED flashed, but the Logic LED remains red.
   Re-install the software and try again (in case of a bad copy of the logic file).
- **No**. The Reset LED does not flash. Contact Nohau Technical Support.

## **Known Device Driver Conflicts**

Nohau is aware of potential device driver conflicts with certain network cards running on Novell/ Netware networks. Problems have been reported with both 3COM ISA network cards and some Novell network cards. Most of these problems have been experienced when running Windows NT or Windows 2000 operating systems.

#### **Possible Symptoms**

- When starting Seehau, communication with the network stops. (You will be unable to access resources on the network.)
- Seehau will not start.

A possible solution might be to change your network card. Nohau Support has not tested all network cards, although some customers have reported that the following network cards have resolved this conflict:

- Intel Ether Express Pro 10/100 ISA
- 3COM Etherlink III (905B or later) 10/100 PCI
- Bay Networks NetGear FA310TX 10/100 PCI

# If the Emulator Does Not Start When Connected to the Target System

- Make sure power is applied to the target system.
- If the target has an external watchdog timer, make sure you do not select **Ext. Reset Enable** in the **Emulator Configuration** dialog box.
- Try switching the crystal jumpers/switches to the Pod position.
- Disconnect the target. Make sure you change the crystal and power jumpers to the Pod position. Then try starting Seehau.
- Check the orientation of the target adapter. Confirm that the adapter is inserted properly. For more information, refer to Chapter 5, "Connecting the Emulator to Your Target Board."
- Check for grounding problems. The emulator and target should have a solid common ground. Targets that are improperly grounded or designed with a *floating* ground might experience improper operation. A closer examination of control signals might reveal excessive over / undershoot or ground noise.
- If you are able to start the emulator, the problem is with one or more of the following critical target signals:
  - address and data bus
  - R/W signal

• Check the address/data bus loading. If your target design approaches maximum fanout for CPU drive capability, the emulator might not function correctly. This is caused by additional loads (approximately two TTL loads) from the pod board.

## **Target Does Not Operate Correctly**

Problem:	Serial port is not operating correctly.					
Cause/ Solution:	<ul> <li>Check jumpers on pod board for external crystal selection.</li> <li>Check signal and ground connections between pod and target.</li> </ul>					

Problem:	Cannot access target memory or memory mapped I/O.
Cause/ Solution:	<ul> <li>Check the Memory Map Configuration tab to ensure that the memory address range is mapped to target.</li> </ul>
	<ul> <li>Check that the External Data Ram option is enabled (from the Config menu, select Emulator).</li> </ul>

## Appendix A. I/O Register Maps

I/O number is for I/O commands. Data space addresses equal I/O number plus \$20.

I/O #	I/O Register	Tiny12	2313	2333, 4433	4414, 8515	4434,8535
\$3F	SREG	70	70	70	70	70
\$3E	SPH	_	_	-	70	1, 0
\$3D	SPL	-	70	70	70	70
\$3C	-	-	-	-	_	_
\$3B	GIMSK	6, 5	7, 6	7,6	7, 6	7, 6
\$3A	GIFR	6, 5	7,6	7, 6	7, 6	7, 6
\$39	TIMSK TIMSK	1	7, 6, 3 ,1 _	7, 6, 3 ,1 _	75, 3 ,1 _	_ 72, 0 <sup>4</sup>
\$38	TIFR TIFR	1 _	7, 6, 3 ,1 _	7, 6, 3 ,1 _	75, 3 ,1 _	_ 72, 0 <sup>5</sup>
\$37	_	_	-	-	_	-
\$36	-	_	_	-	_	_
\$35	MCUCR MCUCR MCUCR	64, 1, 0 	_ 50 _	50 	- 70 -	- - 60 <sup>6</sup>
\$34	MCUSR	30	_	30	_	1, 0
\$33	TCCR0	20	20	20	20	20
\$32	TCNT0	70	70	70	70	70
\$31	OSCCAL	70	-	-	_	_
\$30	-	-	-	-	_	_
\$2F	TCCR1A	-	7, 6 ,1, 0	7, 6 ,1, 0	74, 1, 0	74, 1, 0
\$2E	TCCR1B	-	7, 6, 30	7, 6, 30	7, 6, 30	7, 6, 30
\$2D	TCNT1H	-	70	70	70	70
\$2C	TCNT1L	-	70	70	70	70
\$2B	OCR1AH	-	70	70	70	70
\$2A	OCR1AL	-	70	70	70	70
\$29	OCR1BH	-	-	-	70	70
\$28	OCR1BL	-	-	-	70	70
\$27	ICR1H	_	_	70	_	70
\$26	ICR1L	_	-	70	_	70
\$25	ICR1H TCCR2		70		70	_ 60

## I/O Register Valid Bits

I/O #	I/O Register	Tiny12	2313	2333, 4433	4414, 8515	4434,8535
\$24	ICR1L TCNT2		70		70	_ 70
\$23	OCR2	_	-	_	_	70
\$22	ASSR	_	_	_	_	30
\$21	WDTCR	40	40	40	40	40
\$20	-	-	-		_	_
\$1F	EEARH	-	-	-	01	0 <sup>1</sup>
\$1E	EEARL	50	60	70 <sup>2</sup>	70	70
\$1D	EEDR	70	70	70	70	70
\$1C	EECR	30	20	30	20	30
\$1B	PORTA	_	_	_	70	70
\$1A	DDRA	_	_	_	70	70
\$19	PINA	-	-	-	70	70
\$18	PORTB	40 <sup>3</sup>	70	50	70	70
\$17	DDRB	50	70	50	70	70
\$16	PINB	50	70	50	70	70
\$15	PORTC	-	-	50	70	70
\$14	DDRC	-	-	50	70	70
\$13	PINC	_	-	50	70	70
\$12	PORTD	-	60	70	70	70
\$11	DDRD	-	60	70	70	70
\$10	PIND	-	60	70	70	70
\$0F	SPDR	_	-	70	70	70
\$0E	SPSR	_	_	7, 6	7, 6	7, 6
\$0D	SPCR	_	-	70	70	70
\$0C	UDR	_	70	70	70	70
\$0B	USR	_	73	73	73	73
\$0A	UCR	_	70	70	70	70
\$09	UBRR	-	70	70	70	70
\$08	ACSR	73, 1, 0	7, 50	70	7, 50	7, 50
\$07	ADMUX	-	-	6, 20	-	20
\$06	ADCSR	-	-	70	-	70
\$05	ADCH	-	-	1, 0	_	1, 0
\$04	ADCL	_	_	70	_	70

I/O #	I/O Register	Tiny12	2313	2333, 4433	4414, 8515	4434,8535
\$03	-	-	-	-	-	-
\$02	-	-	-	_	-	-
\$01	-	-	-	-	-	-
\$00	-	_	_	_	_	_

### **Table Notes**

- 1. EEARH, does not exist for 4414.
- **2.** EEARL, bits 7..0 for 4433, bits 6..0 for 2333.
- **3.** PORTB, output Port 5 not writable. PB5 will only pull low (open drain) if ddr5 selects it an an output.
- **4.** TIMSK bits for 4434/8535:

7	6	5	4	3	2	1	0
OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	Ι	TOV0

TIMSK bits for all others:

7	6	5	4	3	2	1	0
TOIE1	OCIE1A	OCIE1B	Ι	TICIE1	Ι	TOIE0	-

**5.** TIFR bits for 4434/8535:

7	6	5	4	3	2	1	0
OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	-	TOV0

TIFR bits for all others:

7	6	5	4	3	2	1	0
TOV1	OCF1A	OCF1B	Ι	ICF1		TOV0	-

**6.** 4434/8535 MCUCR bits 6, 5, 4 have the following functions respectively; SE, SM1, and SM0. The others have bits 5 and 4 with the following functions respectively; SE and SM. 4414/8515 bits 7 and 6 have the following functions respectively; SRE and SRW.

## **Register Bit Names**

	I/O Register	Bit Positions							
I/O #		7	6	5	4	3	2	1	0
\$1C	EECR	_	_	_	_	EERIE	EEMWE	EEWE	EERE
\$0E	SPSR	SPIF	WCOL	_	_	-	_	_	-
\$0D	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
\$0B	USR	RXC	TXC	UDRE	FE	OR	_	-	_
\$0A	UCR	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8
\$08	ACSR	ACD	AINBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0
\$07	ADMUX		ADCBG	-	-	-	MUX2	MUX1	MUX0
\$06	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0
\$3F	SREG	I	Т	Н	S	V	Ν	Z	С
\$3B	GIMSK	INT1	INT0	PCIE	-	-	-	-	-
\$3A	GIFR	INTF1	INTF0	PCIF	_	-	_	_	-
\$39	TIMSK TIMSK <sup>1</sup>	TOIE1 OCIE2	OCIE1A TOIE2	OCIE1B TICIE1	OCIE1A	TICIE1 OCIE1B	TOIE1	TOIE0	TOIE0
\$38	TIFR TIFR <sup>1</sup>	TOV1 OCF2	OCF1A TOV2	OCF1B ICF1	OCF1A	ICF1 OCF1B	TOV1	TOV0	TOV0
\$35	MCUCR <sup>2</sup> MCUCR <sup>3</sup> MCUCR <sup>1</sup>	_ SRE _	PUD SRW SE	SE SE SM1	SM SM SM0	– ISC11 ISC11	– ISC10 ISC10	ISC01 ISC01 ISC01	ISC00 ISC00 ISC00
\$34	MCUSR	-	-	-	_	WDRF	BORF	EXTRF	PORF
\$33	TCCR0						CS02	CS01	CS00
\$2F	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	_	-	PWM11	PWM10
\$2E	TCCR1B	ICNC1	ICES1	-	-	CTC1	CS12	CS11	CS10
\$25	TCCR2	_	PWM2	COM21	COM20	CTC2	CS22	CS21	CS20
\$22	ASSR	_	_	_		AS2	TCN2UB	OCR2UB	TCR2UB
\$21	WDTCR	—	_	_	WDTO E	WDE	WDP2	WDP1	WDP0

Notes:

- 1. 4434/8535 only
- **2.** Tiny12 only
- **3.** 2313, 2333/4433, 4414/8515

## **Appendix B. CPU Memory Sizes**

	Flash (Words)	EEPROM (Bytes)	Internal RAM (Bytes)	External RAM (Bytes)	Stack Pointer	Atmel Adapter
2313	1K	128	128	_	8-bit	3300
2333	1K	128	128	_	8-bit	3200
4433	2K	256	128	_	8-bit	3200
4414	2K	256	256	64K	16-bit	3000
8515	4K	512	512	64K	16-bit	3000
4434	2K	256	256	_	10-bit	3100
8535	4K	512	512	_	10-bit	3100
Tiny12	512	64	0	_	Hardware	3400

## Appendix C. 8515 Memory Map

(RAM/data space)

\$FFFF  \$260	External RAM 64,928 bytes	Usable External RAM			
\$25F  \$60	Internal RAM 512 bytes				
\$5F  \$20	I/O Registers	Un-usable External RAM overlaps internal RAM and registers.			
\$1F  0	r0r31				

#### Note

POD–AVR mapping resolution is 256 bytes per block. \$300 is the first address that can be mapped to external memory.

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