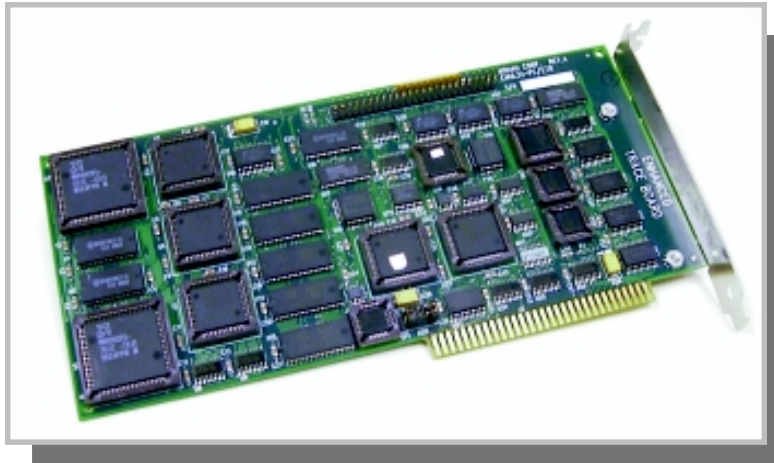# Advanced Trace Board (ATR)
Enhanced Trace Board (ETR)
for Nohau EMUL68-PC and EMUL51-PC In-Circuit Emulators

Background

8051 Trace Options:

The Nohau EMUL51-PC emulator system can use the Standard, Advanced or Enhanced trace cards. These are ISA cards that plug into your PC or the Nohau HSP box. The trace is optional and can be added later to your Nohau emulator system.

HC11 Trace Options:

The Nohau EMUL68-PC can use the Standard and Enhanced trace option. The trace is optional as in the 8051 emulator and can be added later.

The various trace cards can be added or upgraded to your Nohau emulator system to give advanced trace functions and increase your productivity.

Key Benefits of Advanced Trace Cards (ATR)

♦ Works with Nohau debuggers for DOS, Windows GUI, Seehau and also ChipView ChipTools for the 8051.

♦ Trace FIFO memory available in 64K or 256K models.

♦ Event Timer: 16 bit timestamp with 16 bit prescaler.

♦ 8 complex event triggers find specified events quickly on data read/write and opcode execution. Each of these eight qualifiers are enhanced with the 6 bit State machine and special Boolean Processing to provide you with a 64 Level Trigger qualifier system.

♦ Banking is supported.

♦ Operates at all Nohau emulator speeds.

♦ Trace and triggers are viewed and modified in real-time & "on-the-fly". No CPU cycles are stolen for these operations.

Key Benefits of Enhanced Trace Cards (ETR)

The Advanced Trace card benefits plus:

♦ 64K Shadow RAM displays CPU writes in real-time without stealing cycles from your program.

♦ Trace memory in 64K or 256K deep FIFO models.

♦ Event Timer: 32 bit timestamp with 16 bit prescaler.

♦ Code Coverage shows accesses in various memory areas.

8051 Code Coverage Options

The Code Coverage displays memory areas accessed in these modes:

1) program code fetch access.
2) program memory first byte fetch.
3) read cycles from external data memory (XDATA).
4) write cycles to external data memory (XDATA).

HC11 Code Coverage Options

The Code Coverage feature displays those memory areas accessed in these modes:

1) all memory accesses.
2) Instruction fetch (LIR active).
3) read cycles.
4) write cycles.

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Cut Development Time

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